REMARKS

Applicants respectfully request reconsideration of a prior art rejections set forth by the Examiner under 35 U.S.C. sections 102 and 103 Applicants respectfully submit that the prior art references of record, whether considered alone, or in combination, fail to either teach or suggest Applicants presently claimed invention. Applicants presently claimed invention is directed to the formation of a pseudo-wafer that advantageously improves the efficiency of the manufacturing process by enabling batch processing of a number of good semiconductor chips in a single wafer structure.

As described in the instant application, a plurality of good semiconductor chips are applied to a sheet of adhesive material that may be secured over a quartz substrate. Resin is thereafter applied to surfaces of the individual semiconductor chips that have been applied to the adhesive sheet of material to cover sides of the chips other than the side surface at which the electrodes for the chip are located. Thereafter, the adhesive sheet and the wafer substrate are eliminated to thereby provide a pseudo-wafer formed of the resin body containing a plurality of chips. This pseudo-wafer may be conveniently used for batch processing of the semiconductor chips for the formation of such structures as the solder balls and electrical connections to the individual semiconductor chips.

In contrast with the newly cited Camien reference, the prior art describes the use of an epoxy material and placement of individual chips in a potting tool. The new prior art reference indicates that the silicon dies are placed face down on a drop of epoxy in the potting tool and additional epoxy is poured over the back of the dies. See, for example, column 4 beginning at line 30. As described in column 5 at line 8, once the re-wafering

process has been completed in the prior art, the wafer is removed from the potting tool and the wafer is held with the active face of the die up so that subsequent necessary processing is performed on that surface. As described therein, the prior art teaches the application of a passivation layer directly to the circuit face of the wafer. This contrasts with Applicants presently claimed invention wherein a layer of silicon dioxide is initially applied prior to the use or formation of any passivation layer.

Applicants respectfully submit that the references cited by the Examiner do not teach or suggest Applicants presently claimed invention wherein both silicon dioxide and a further passivation layer is applied to the electrode side of a pseudo-wafer. Applicants further submit that the remaining references of record are similarly deficient and fail to provide any teaching or suggestion whatsoever regarding both the formation of the pseudo-wafer structure as specified and the formation of various electrode structures including the insulating material such as the silicon dioxide and passivation layer has now specified.

Applicants further note that the primary reference relied upon by the Examiner is intended provide stackable IC chips or die layers which permit chips having different functions and different physical areas to be stacked as if they were the same size chips. This is substantially different than Applicants presently claimed invention wherein multiple chips, which may be of the same size or different size, are secured into a common wafer for batch processing. The batch processing is used to provide the formation of electrode structures and the like.

In light of the foregoing, Applicants respectfully submit that the prior art fails to teach or suggest Applicants invention is now specified. Accordingly, Applicants submit that all claims now standing condition for allowance.

Respectfully submitted,

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(Reg. #37,607)

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